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(54) Drahtlose Übertragungseinrichtung mit einem Lautsprechersystem

English translation

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WIRELESS TRANSMITTING MEANS INCLUDING A SPEAKER SYSTEM

The present innovation relates to a wireless transmitting means including a speaker system, especially a wireless transmitting means including a speaker system, which is able to transmit audio signals simultaneously from a left (L) and a right (R) audio channel through various channels to a speaker for emission of sounds.

Figure 1 shows a wireless transmitting means having a speaker system according to the prior art, including a transmitting unit 80 and a receiving unit 90. In the transmitting unit 80, the audio signals of the left (L) and the right (R) are modulated by means of a multiplexer 81. Subsequently, the modulated signal is sent to an antenna 83 by means of a transmitting module for radio frequencies in order to be emitted from there.

The receiving unit 90 receives the signal from the transmitting unit 80, passes the received signal to a demultiplexer 93 by means of a receiver module 92 for radio frequencies for demodulation such that the original left and right audio signals are again obtained.

Accordingly, it is the object of the present innovation to provide a wireless transmitting means including a speaker system, wherein the right/left audio signals are detected by a microprocessor, which then controls the frequency of the radio frequency channel, and which specifies the left and right audio frequencies of the receiving and the transmitting end. Further, it is the object of the present innovation to provide a wireless transmitting means including a speaker system, wherein arising of a too high level of the audio signal is prevented. The sound quality is not to be affected by environmental influences.

Further various objects and advantages of the present innovation are directly apparent from the following detailed description together with the appended drawing. There show:

Figure 1 a circuit block diagram of a wireless transmitting means including a speaker system according to the prior art.

Figure 2 a circuit block diagram of the transmitting means according to the present innovation;

Figure 3 the circuit of the transmitting means according to the present innovation;

Figure 4 the circuit block diagram of the circuit unit in the receiver unit of the present innovation;

Figures 5 and 6 the circuit diagrams of the receiver unit according to the present innovation;

Figures 7 and 8 flow diagrams of the internal program of the microprocessor in the receiving unit of the present innovation.

By way of figures 2 to 6, the wireless transmitting means including a speaker system according to the present innovation is illustrated in greater detail. The wireless transmitting means includes a speaker system with a speaker, a transmitting unit 1, a receiving unit 2, and at least one speaker 3.

The transmitting unit 1 is formed of a voltage supply 11, a voltage regulator 12, a microprocessor 13, a radio frequency transmitting module 14, a level control circuit 15 and a transmitting antenna 16.

The voltage supply 11 (adapter) serves for passing its output voltage to the voltage regulator 12 in order to supply it (12) with the necessary operating voltage.

The voltage regulator 12 is formed of a voltage regulator circuit U1, a switch S1, resistors R12, R1 and R4, capacitors C1, C2, C3, C4 and C5, a light emitting diode LED1, a Zener diode ZD5, a diode 5, and further components. Its output is connected to the microprocessor 13 and to the radio frequency transmitting module 14.

The voltage regulator 12 serves for regulating the output voltage of the voltage supply 11 to obtain a DC voltage of 5 V, in order to thus supply the microprocessor 13 and the radio frequency transmitting module 14 with the necessary operating voltage.

The radio frequency transmitting module 14 is formed in that a modulator circuit T1, an edge connector CN1 and further parts are connected to each other. Its input is

connected to a level control circuit 15 formed of the resistors R9 and R10, a variable resistor VR1, capacitors C11 and C12, diodes D1 and D4, Zener diodes ZD1 through ZD4, and further components, wherein the variable resistor VR1, the diodes D1 and D4, the Zener diodes ZD1 through ZD4 are formed as a blocking circuit. The blocking circuit is used for level limitation to avoid a too high audio output level and to achieve accordingly a required protecting effect. The output of the modulator circuit T1 is connected to a transmitting antenna 16.

The microprocessor 13 is formed of an integrated circuit U2, resistors R2, R3, R5, R6, R7, R11, capacitors C9, C10, C13 etc. Data lines SCL, SDA and a control line EN of the integrated circuit U2 are connected to the radio frequency transmitting module 14. The inputs/outputs of the microprocessor 13 are connected to a switch S2 through which four channels are selectable.

The microprocessor 13 causes the switch S2 to switch to a selected channel such that the radio frequency transmitting module 14 modulates the input audio signal of the various channels and then emits the modulated signal via the transmitting antenna 16.

In figures 4 and 5, the receiving unit 2 is formed of a voltage supply 21, a voltage regulator 22, a microprocessor 23, a radio frequency receiving module 24, a display 25 for the receive strength of the input signal, a receiving antenna 26 and an amplifier 17.

The voltage supply 21 (adapter) serves for supplying its output voltage to the voltage regulator 22 and to the amplifier 27 in order to supply the voltage regulator 22 and the amplifier 27 with the necessary operating voltage.

The voltage regulator 22 is formed of a voltage regulator circuit U1, a switch S1, resistors R1, R2, capacitors C1, C2, C3, C4, C5, a light emitting diode LED2, a Zener diode ZDL, a diode D1, and further components. Its output is connected to the microprocessor 23 and to the radio frequency receiving module 24.

The voltage regulator 22 serves for regulating the output voltage (15 V DC voltage) of the voltage supply 21 to derive a DC voltage of 5 V therefrom, in order to thereby supply the microprocessor 23 and the radio frequency receiving module 24 with operating voltage.

The radio frequency receiving module 24 is formed of a modulator circuit C2, an edge connector CN3 and further components. Its input is connected to the receiving antenna 26. Its output is connected to a variable resistor VR controlling the volume. The variable resistor VR is connected to an amplifier 27, formed of a circuit U4, transistors Q1 and Q2, resistors R40 to R54, capacitors C40 to C51, and further parts. The amplifier output is connected to the speaker 3.

The microprocessor 23 is formed of a circuit U3, resistors R3 to R8, capacitors C9 to C10, and further components. It is connected to the radio frequency receiving module 24 by means of data lines SCL, SDA and a control line 231 (EN). The line 232 for muting is connected to the amplifier 27. The inputs/outputs of the microprocessor 23 are connected to switches S4 and S5. The switch S4 has 4 channels, while the switch S5 serves for selecting the right/left audio signal.

With the aid of the internal program, the microprocessor 23 determines the switch positions of the switches S4

and S5, controls the frequency of the radio frequency channel for a decision "right or left audio channel" of the receiving or transmitting ends. Subsequently, the radio frequency receiving module 24 receives the signals from the receiving antenna 26 and demodulates them. Thereupon, the demodulated signals are output to the amplifier 27 for amplification. Finally, the speaker 3 emits the appropriate sounds.

Additionally, a receive strength display 25 for the receive signal (RSSI) is connected between the radio frequency receiving module 24 and the microprocessor. The receive strength display 25 for the receive signal is formed of operational amplifiers U4A and U4B, resistors R11 to R14, capacitors C14, C15, C17 etc.

The receive strength display 25 for the receive signal derives a signal indicating the field intensity of the carrier signal from the radio frequency receiving module 24. By means of this signal, the sound quality affected by environmental factors is determined. If the quality of the audio signal is worse than a preset value, the microprocessor 23 mutes the speaker 3.

Figure 7 shows a flow diagram of the program stored in the microprocessor 23 of the receiving unit 2 of the present innovation. First, it is determined if the frequency is 900 MHz or 863 MHz (step 50).

If the frequency is 863 MHz, the display is set to 863 MHz (step 501) and the frequency is clamped (step 51). If the frequency is 900 MHz, the display is set to 900 MHz (step 502) and the frequency is clamped (step 51). Subsequently, it is checked if the channel has been changed (step 52).

If not, this detection operation is continued, otherwise it is determined if the channel is a transmitting channel or a receiving channel (step 53).

If the channel is a transmitting channel, the address 531 of the left audio channel is read and the read datum is sent to a channel changing subroutine of the program to perform an action. After performing the action, the right sound channel address 533 is sent to the channel changing subroutine to perform a necessary action. After this action, the method returns to step 52. If the channel is a receiving channel, the method determines if it is a left or a right channel (step 54).

If the channel is a right channel, the method reads a received address 541 for the right audio channel and transmits the read data to the channel changing subroutine to perform the appropriate action. After completing this action, the method returns to step 52. If the channel is a left channel, the method reads the received address 542 of the left audio channel and transmits the read data to the channel changing subroutine to perform a necessary action. After this action, the method returns to step 52.

Figure 8 shows the flow diagram for the change of channel. First, the method determines if the selected channel is the first channel (step 70).

If so, it is determined if the frequency of the channel is 900 MHz or 863 MHz (step 73). Otherwise, the address is incremented by 3 (step 701). Thereafter, it is determined if the selected channel is the second channel (step 71).

If so, the method continues with step 73. Otherwise, the address is incremented by 3 (step 711). Subsequently, it

is determined if the selected channel is the third channel (step 72).

If so, the method proceeds to step 73. Otherwise, the address is incremented by 3 (step 721). Thereafter, it is determined if the frequency of the channel is 900 MHz or 863 MHz (step 73).

If the frequency is 863 MHz, the value 40H is added to the address in step 731. Subsequently, any value of the address table is read (step 732). Otherwise, if the frequency is 900 MHz, any value in the address table is directly read (step 732). Subsequently, according to the address value, data are sent to the radio frequency receiving part 24 (step 733). Thereupon, the method returns to the main program.

Therefore, by means of the special circuitry described above, using wireless transmission, the signals incoming from the left (L) or right (R) channel are split to various channels and transmitted to the speaker 3 for sound emission. A too high audio input signal is avoided and the sound quality is unaffected by the exterior environment.

Although the present innovation is described with respect to the preferred embodiments, it is understood that the innovation is not limited to the described details. Various alternatives and modifications have been proposed in the above description, and one skilled in the art will be able to also recognize additional other ones. Therefore, all of such alternatives and modifications are part of the scope of the present innovation as defined in the appended claims.

C l a i m s :

1. Wireless transmitting means including a speaker system comprising the features of:

at least one speaker (3),

a transmitting unit (1) for simultaneously transmitting audio signals of a left (L) and a right (R) audio channel through various channels,

a receiving unit (2), the receiving unit (2) including:

- an input voltage supply to supply the receiving unit (2) with operating voltage,

- a receiving antenna (26) for receiving the signal from the transmitting unit (1),

- a radio frequency receiving module (24) connected to the receiving antenna (26), the output of which is

connected to an amplifier (27), the output of the amplifier (27) being connected to the speaker (3),

- a microprocessor (23) connected to the radio frequency receiving module (24) and accordingly to the amplifier (27), wherein the inputs/outputs of the microprocessor (23) are connected to a first (S4) and a second switch (S5), wherein a channel is selectable from a number of selectable channels with the first switch (S4), and wherein the second switch (S5) serves for selecting the right/left audio frequency, wherein the microprocessor (23) determines the states of the first (S4) and the second switch (S5), controls the frequency of the audio frequency channel and determines the left or right audio channel of the receiving and transmitting ends, wherein the radio frequency receiving module (24) demodulates signals from the receiving antenna (26), wherein subsequently the amplifier (27) amplifies these signals and thereupon sends them to the speaker (3) for emission, and

- including a receive strength display (25) for the receive signal connected between the radio frequency receiving module (24) and the microprocessor (23), wherein the receive strength display (25) derives a signal indicating the field intensity of the carrier signal from the radio frequency receiving module (24) for the receive signal, wherein the sound quality affected by environmental factors is determined and the microprocessor (23) mutes the speaker (3) if the sound quality is too poor.

2. Wireless transmitting means including a speaker system according to claim 1, wherein the input voltage supply further has a voltage supply (21), the output of which is connected to the amplifier (27) and to a voltage regulator (22), wherein the voltage regulator (22) serves for regulating the voltage incoming from the voltage supply (21), in order to produce a voltage

therefrom and to thereby supply the microprocessor (23) and the radio frequency receiving module (24) with the necessary operating voltage.

3. Wireless transmitting means including a speaker system according to claim 1, wherein the microprocessor (23) is connected to the radio frequency receiving module (24) by means of data lines SCL, SDA and a control line EN (231).

4. Wireless transmitting means including a speaker system according to claim 1, wherein the microprocessor (23) is connected to the amplifier (27) through a line (232) for muting.

5. Wireless transmitting means including a speaker system according to claim 1, wherein a regulating element (VR) is connected between the radio frequency receiving module (24) and the amplifier (27).

6. Wireless transmitting means including a speaker system according to claim 1, wherein the transmitting unit (1) includes the features of:

an input voltage supply for providing operating voltage required by the transmitting unit (1),

a radio frequency transmitting module (14) connected to the input voltage supply, the output of which is output to a transmitting antenna (16),

including a microprocessor (13) connected to the input voltage supply and accordingly to the radio frequency transmitting module (14), the input/outputs of which are connected to a third switch (S2) for selecting a plurality of selectable channels,

wherein the microprocessor (13) controls the signal frequency of the radio frequency according to the state of the third switch (S2), wherein the radio frequency transmitting module (14) modulates the input audio

signal and wherein the modulated signal is emitted by the transmitting antenna (16).

7. Wireless transmitting means including a speaker system according to claim 6, wherein the transmitting unit (1) additionally includes a level control circuit (15) connected to the input of the radio frequency transmitting module (14), wherein the level control circuit (15) serves for receiving the audio frequencies of the left (L) and the right channel (R) and for thereby avoiding a too high audio signal level.

8. Wireless transmitting means including a speaker system according to claim 6, wherein the input voltage supply further comprises a voltage supply (11), the output of which is connected to a voltage regulator (12), wherein the voltage regulator (12) serves for regulating the voltage output from the voltage supply (11), in order to output a voltage serving as the operating voltage, which is required by the microprocessor (13) and by the radio frequency transmitting module (14).

9. Wireless transmitting means including a speaker system according to any one of claims 1 to 8, wherein the microprocessor (13) is connected to the radio frequency transmitting module (14) by means of data lines SCL, SDA and a control line EN.

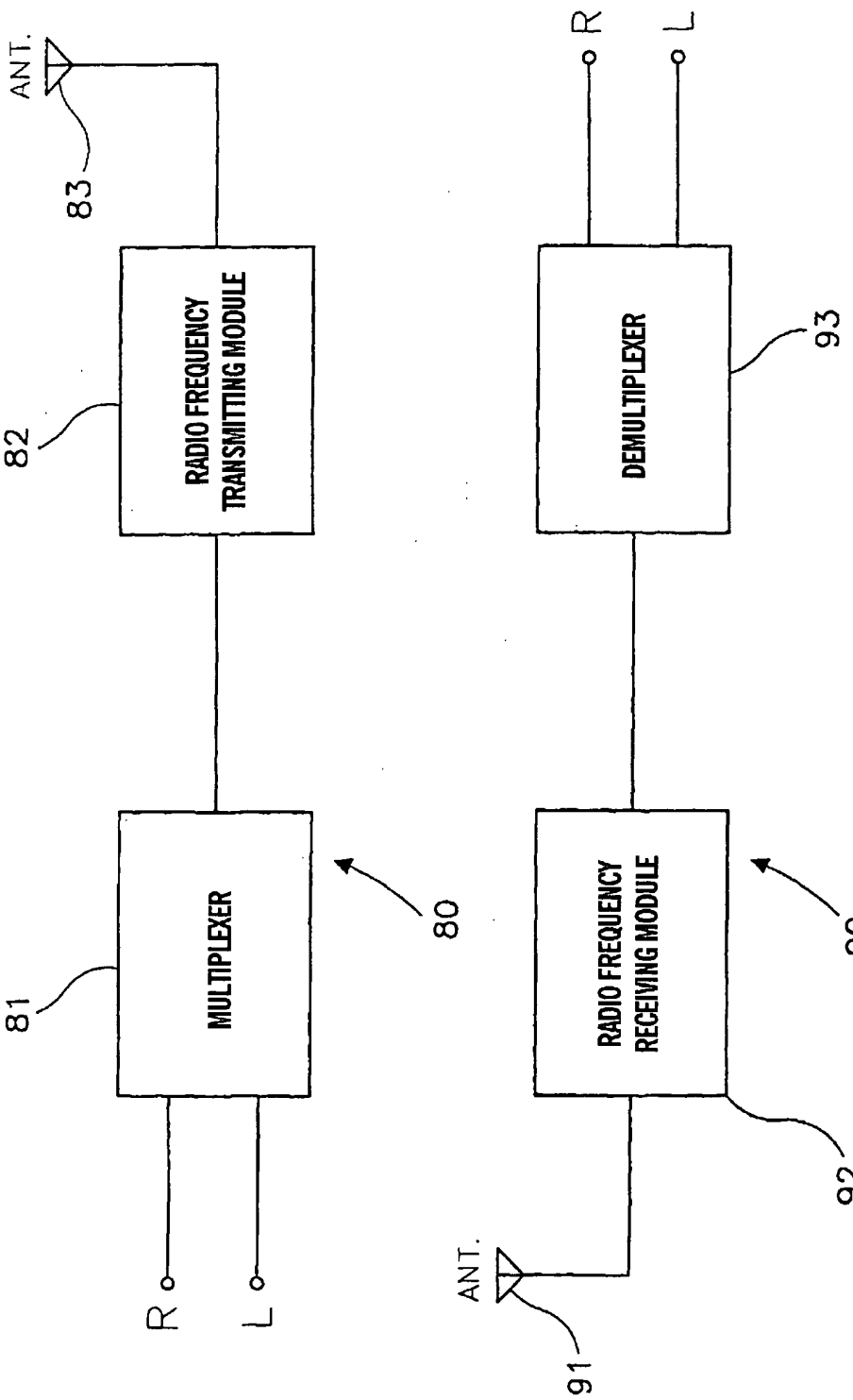
ANT.
83
82
RADIO FREQUENCY TRANSMITTING MODULE
81
MULTIPLEXER
80
R
L
R
L
DEMULTIPLEXER
93
RADIO FREQUENCY RECEIVING MODULE
90
92
ANT.
91

FIG. 1

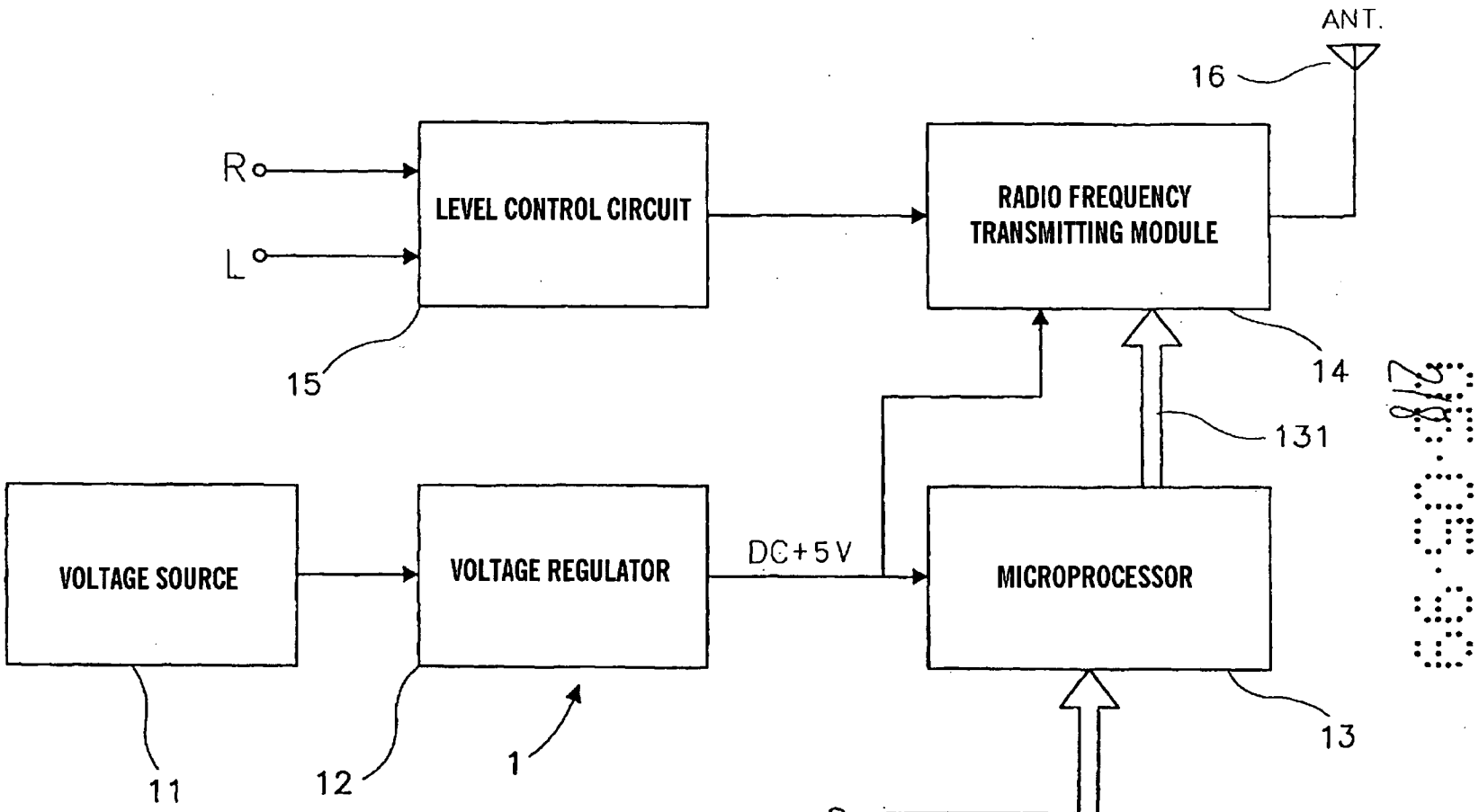
ANT.
16
R
L
LEVEL CONTROL CIRCUIT
RADIO FREQUENCY TRANSMITTING MODULE
15
14
131
VOLTAGE SOURCE
VOLTAGE REGULATOR
DC+5V
MICROPROCESSOR
11
12
1
13
S_2

FIG. 2

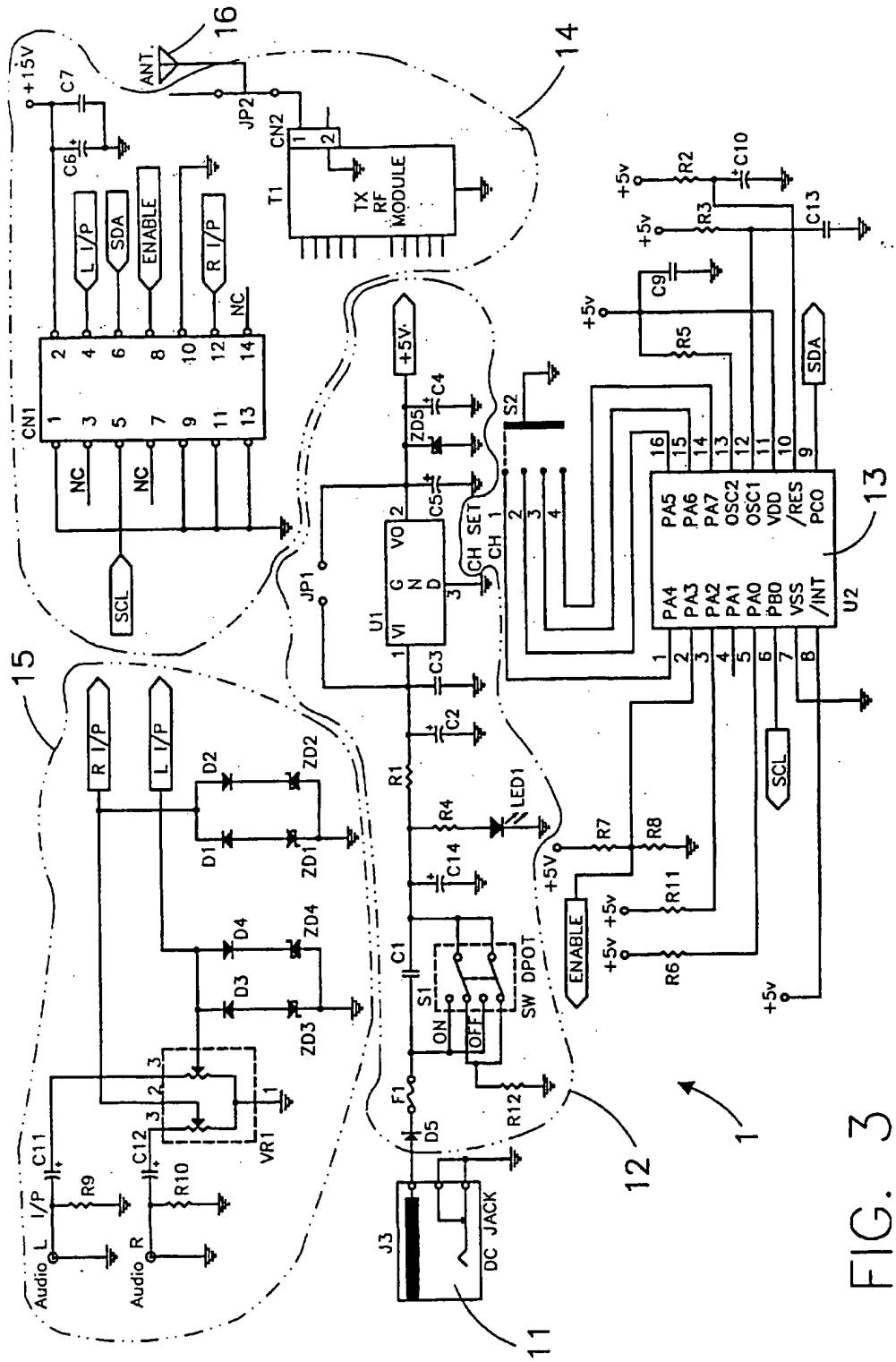
16
14
ANT.
JP2
CN2
T1
TX RF MODULE
+15V
C7
C6
L I/P
SDA
ENABLE
R I/P
NC
CN1
SCL
+5V
C4
ZD5
C5
S2
CH SET
CH 1
JP1
U1
VI
G N D
VO
C3
C2
R1
R4
LED1
C14
C1
S1
ON
OFF
SW DPOT
F1
D5
R12
J3
DC JACK
15
D2
ZD2
D1
ZD1
D4
ZD4
D3
ZD3
VR1
C11
C12
R9
R10
Audio L I/P
Audio R
12
11
+5v
R2
C10
R3
C13
C9
R5
SDA
PA5
PA6
PA7
OSC2
OSC1
VDD
/RES
PCO
PA4
PA3
PA2
PA1
PA0
PB0
VSS
/INT
U2
13
SCL
R7
R8
R11
R6
ENABLE
1

FIG. 3

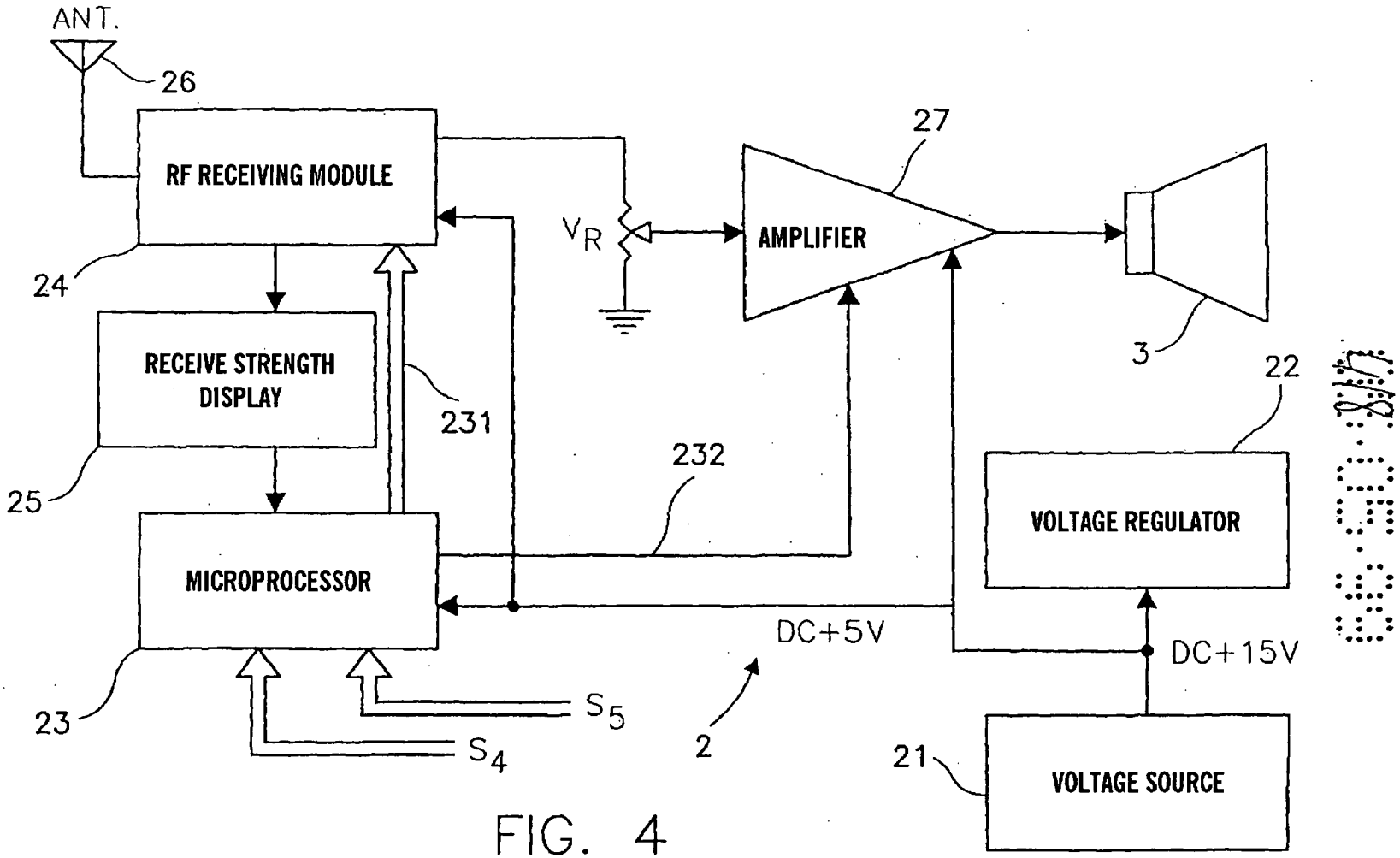
ANT.
26
RF RECEIVING MODULE
24
RECEIVE STRENGTH DISPLAY
25
MICROPROCESSOR
23
231
232
V_R
AMPLIFIER
27
3
22
VOLTAGE REGULATOR
DC+15V
DC+5V
2
S_5
S_4
21
VOLTAGE SOURCE

FIG. 4

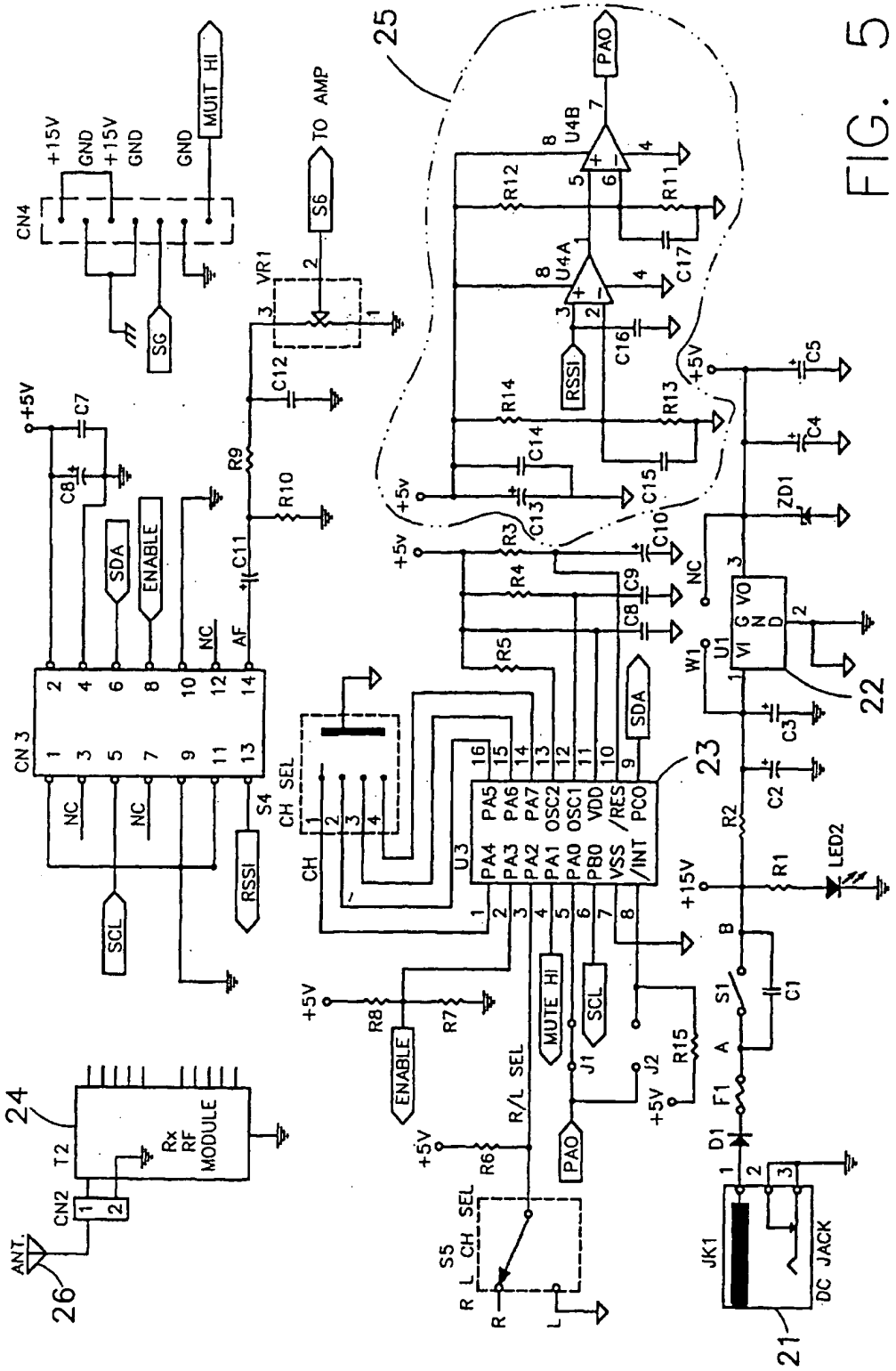
25
PAO
U4B
R12
R11
C17
U4A
C16
RSSI
R14
R13
C14
C15
C13
C10
+5V
R3
R4
C9
C8
R5
NC
ZD1
C5
C4
C3
C2
R2
R1
LED2
W1
U1
VI GND VO
22
23
CH SEL
CH
U3
PA4 PA3 PA2 PA1 PA0 PB0 VSS /INT
PA5 PA6 PA7 OSC2 OSC1 VDD /RES PC0
SDA
MUTE HI
SCL
ENABLE
R8
R7
R6
R/L SEL
J1
J2
R15
S1
C1
F1
D1
JK1
DC JACK
21
CN 3
NC
SCL
RSSI
S4
SDA
ENABLE
C8
C7
+5V
C11
R9
R10
C12
VR1
S6
TO AMP
CN4
+15V
GND
SG
MUIT HI
24
T2
Rx
RF
MODULE
CN2
ANT.
26

FIG. 5

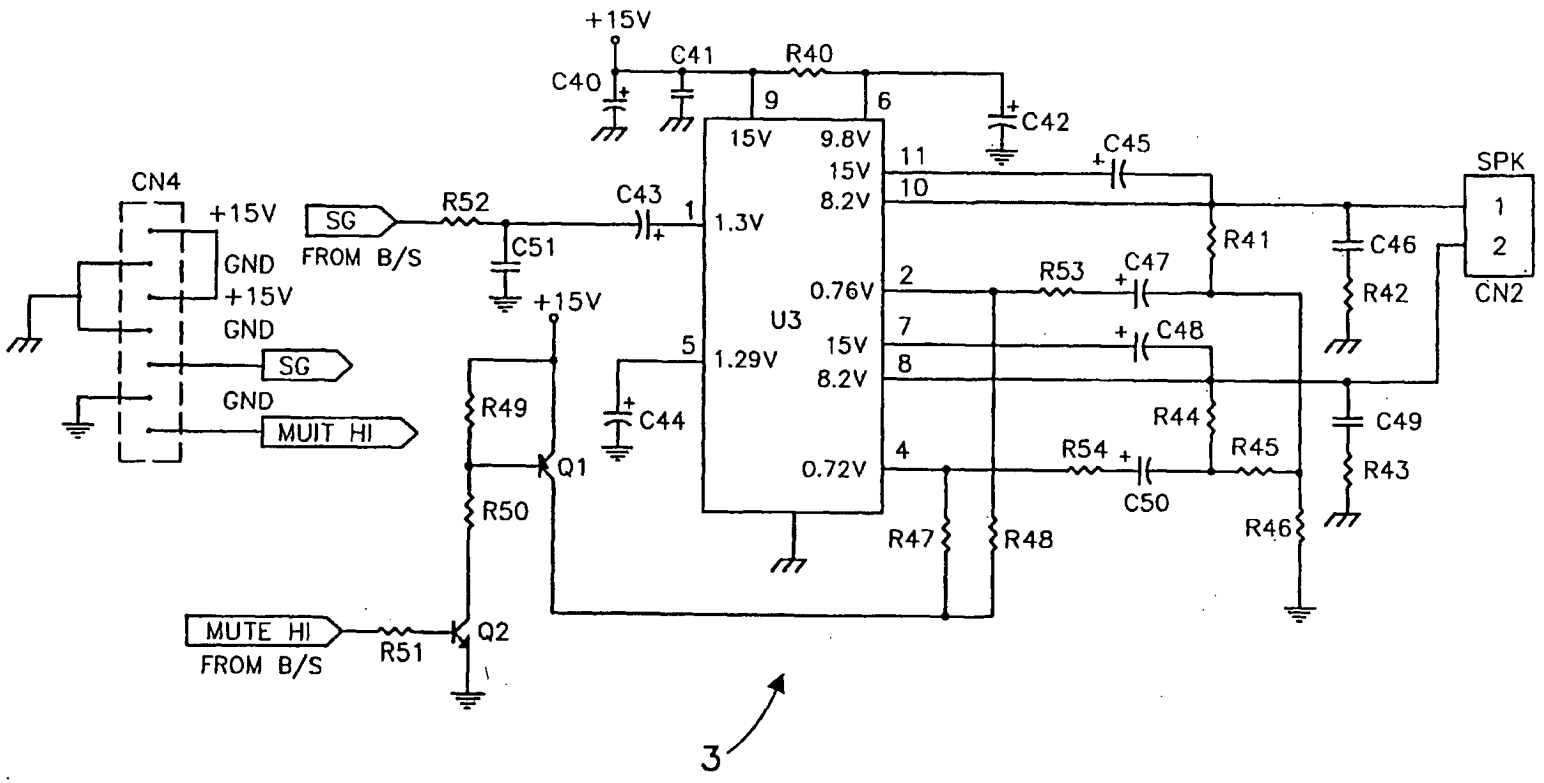
+15V
C40
C41
R40
9
6
C42
15V
9.8V
15V
8.2V
11
10
C45
SPK
1
2
CN2
CN4
+15V
GND
+15V
GND
SG
GND
MUIT HI
SG
FROM B/S
R52
C51
C43
1
1.3V
+15V
U3
0.76V
2
R53
C47
R41
C46
R42
7
15V
8.2V
8
C48
5
1.29V
C44
R49
Q1
R50
0.72V
4
R44
R45
R54
C50
C49
R43
R47
R48
R46
MUTE HI
FROM B/S
R51
Q2
3

FIG. 6

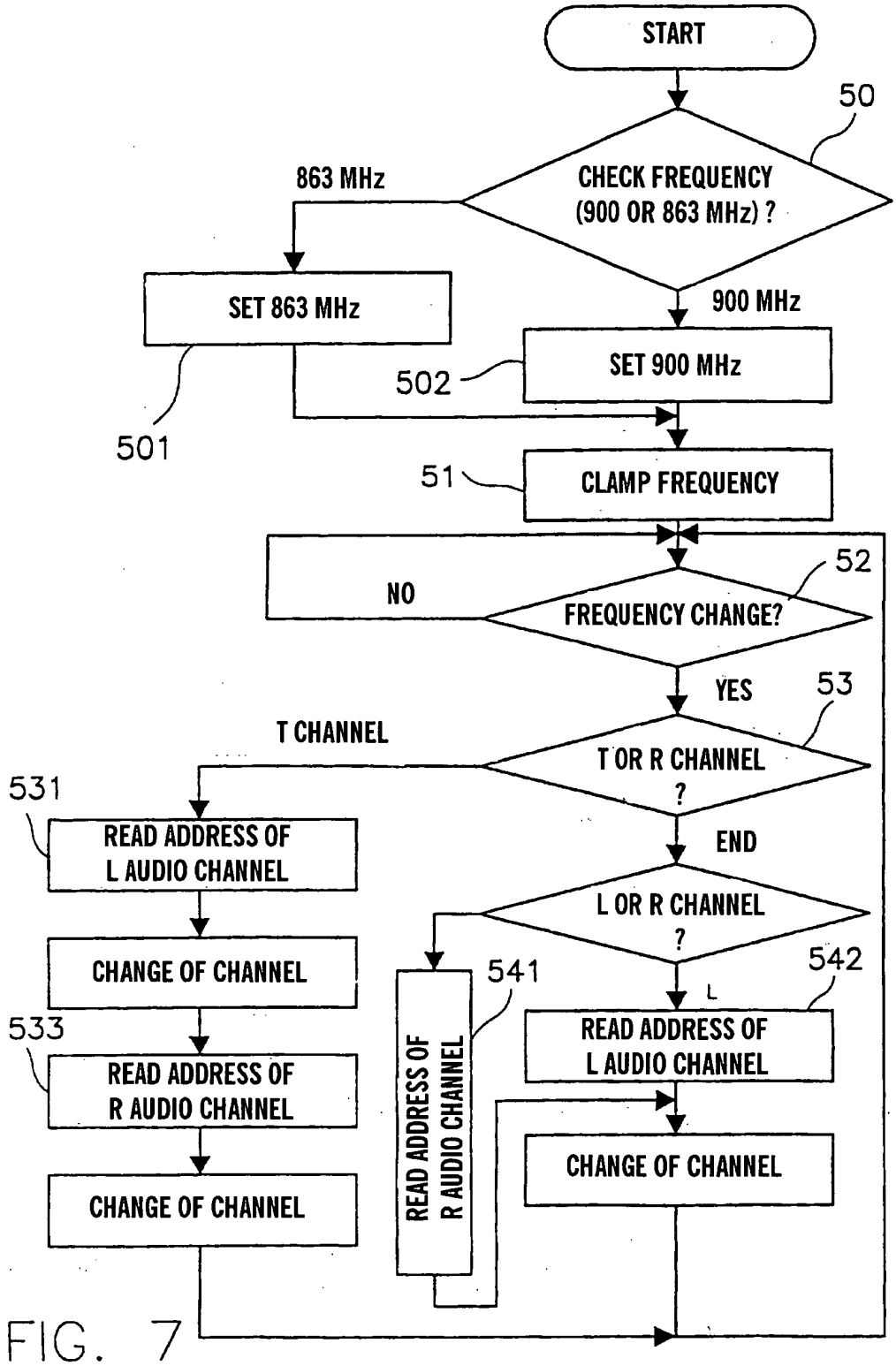

FIG. 7

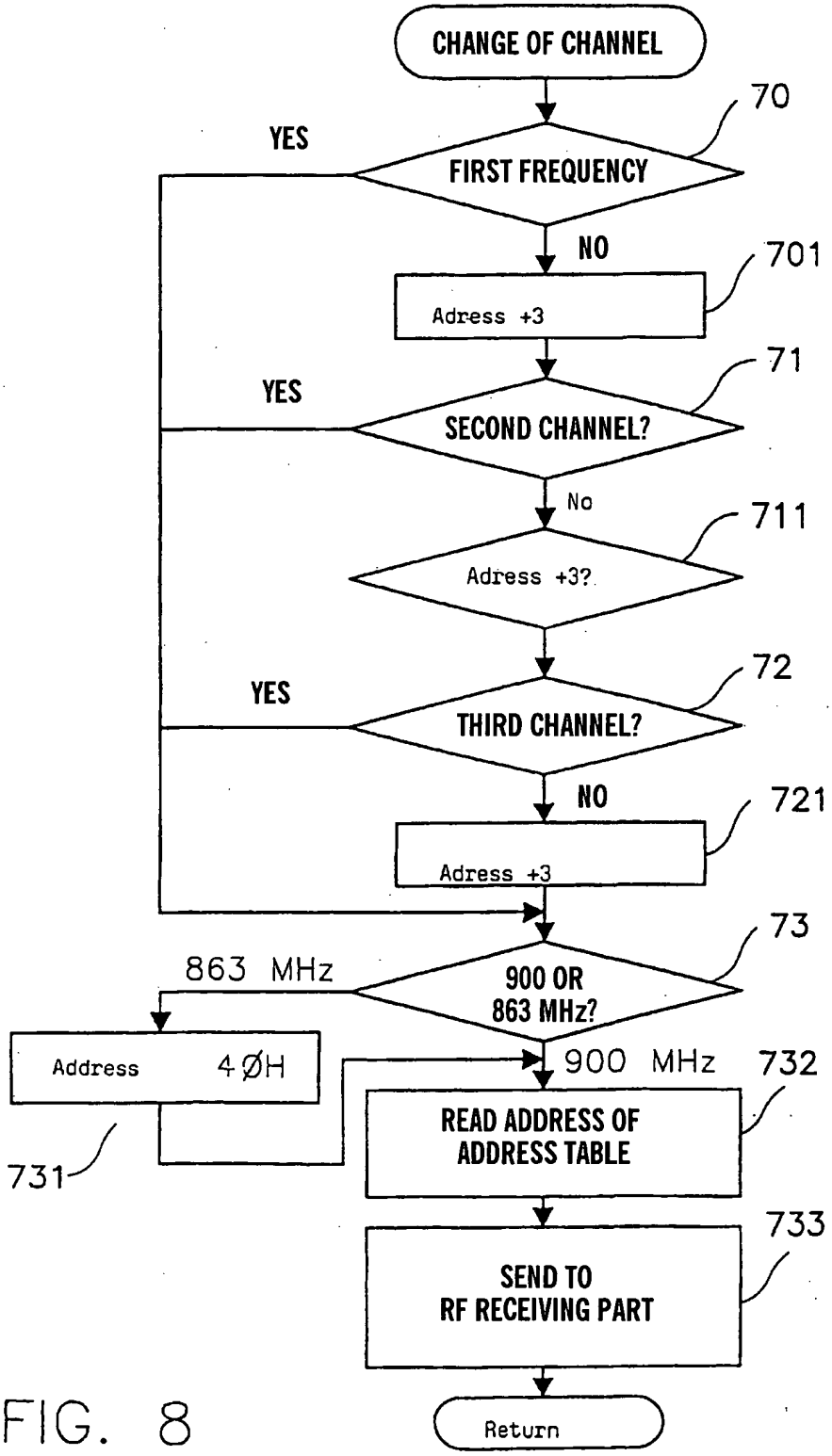

FIG. 8